DIGITAL SYSTEM DESIGN LAB
PCC-ECE405-P

Course Credits: 2 Contact Hours: 4/week, (L-T-P: 0-0-4) Mode: Lab work Examination Duration: 3 hours	**Course Assessment (Internal: 30; External:70)**

Sr. No.	Course Outcomes At the end of the semester, students will be able to:	RBT Level
CO 1	Describe the use of HDLs for VLSI digital system design.	L1
CO 2	Illustrate the various CAD tools available for Digital system design.	L2
CO 3	Demonstrate the importance of HDL and CAD tools in VLSI digital system design.	L3
CO 4	Compare the various design techniques for digital system design.	H1
CO 5	Design and evaluate the performance of digital systems.	H2
CO 6	Develop or create digital system using HDLs and FPGAs.	H3

List of Experiments

1. Familiarization with VHDL/Verilog and CAD tools.
2. Design all digital logic gates using VHDL.
3. Design a half adder digital logic using VHDL.
4. Design a 3-to-8 Decoder using 1-to-2 Decoder using VHDL.
5. Design a 8-to-1 MUX using 2-to-1 MUX using VHDL.
6. Design 1-bit full adder using 2x1 Multiplexer in VHDL.
7. Design a 4-Bit Comparator using VHDL.
8. Design all logic gates and 4-bit Full Adder using VHDL.
9. Design a 4-bit Full Adder-Subtractor using VHDL.
10. Design a 4-bit ALU using VHDL.
11. Design a D-latch D-FF using VHDL.
12. Design register, shifter and counter using VHDL.
13. FPGA implementation of 4bit Counter using VHDL.
14. FPGA implementation of Finite state machine using VHDL.
15. FPGA implementation of 7-segment decoder using VHDL.
16. Write VHDL code to display messages on an alpha numeric LCD display.

NOTE: At least twelve experiments are to be performed out of which at least eight experiments should be performed from above list. The remaining experiments may be performed from the above list or designed and set by concerned institution as per the scope of the syllabus.